* R N - 8 0 6 5 / 3 0 0 *

RN-8065

B. E. II (Sem. III) (EC/CO/IT/IC) Examination

May / June – 2010

Digital Logic Design

Time : **3** Hours] [Total Marks : **100**

Instruction :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. 2 (Sem. 3) (EC/CO/IT/IC)**

Name of the Subject :

☛ **Digital Logic Design**

☛ Subject Code No. : **8 0 6 5** ☛ Section No. (1, 2,.....) : **1&2**

Seat No. :

Student's Signature

(2) Attempt **all** questions.

(3) Assume suitable data whenever **necessary**.

(4) Figures to the **right** indicate full marks.

SECTION - I

1 (a) Answer following questions : **10**

(i) Convert $(0.6234)_{10}$ into its equivalent octal number.

(ii) Subtract $(9)_{10}$ from $(4)_{10}$ using 1's complement method.

(iii) Find the excess-3 code and its 9's complement for $(592)_{10}$.

(iv) Prove $A + \bar{A}B = A+B$

(v) Define an integrated circuit. Also give classification of digital ICs.

(b) (i) Obtain an 8:1 MUX using two 4:1 MUX. **5**

(ii) Simplify the following equation using K-map **5**

$f(A, B,C,D,E) = \sum m (0, 2, 5, 7, 13, 15, 18, 20, 21, 23, 28, 29, 31)$

2 (a) Simplify the following using tabulation method. **8**

$Y (w, x, y, z) = \sum m (1, 2, 3, 5, 9, 12, 14, 15) + \sum d (4, 8, 11)$

(b) Explain parity checker with truth table, K-map simplification and logic diagram. **7**

OR

2 (a) A combinational circuit is defined by the functions : **8**

$F_1 = \sum m (3,5,7)$

$F_2 = \sum m (4,5,7)$

Implement the circuit with a PLA having 3 inputs, 3 product terms and two outputs.

(b) Realize the following expression using only NOR gates. **4**

$Y = (ABC + \overline{B}\overline{C})\ C$

(c) Draw and explain timing diagrams and pin configuration of IC 7402. **3**

3 Write short notes on any **three** : **15**

(i) BCD to 7 segment code converter

(ii) ROM

(iii) Internal block diagram of a digital computer

(iv) 4-bit magnitude comparator.

SECTION - II

4 (a) Give answer in short : **10**

(i) Give the definition of the propagation delay and setup time.

(ii) Give characteristics table and excitation table for D flip flop.

(iii) For edge trigger T flipflop, as given in figure 1, draw output wave form.

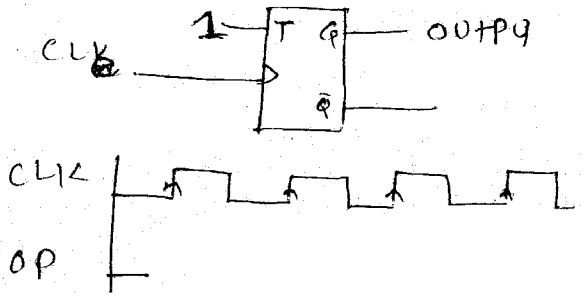

Fig. 1

(iv) Explain face condition and solution on it.

(v) Draw olp wave for Fig. 2 flipflop used here negative edge trigger D flipflop.

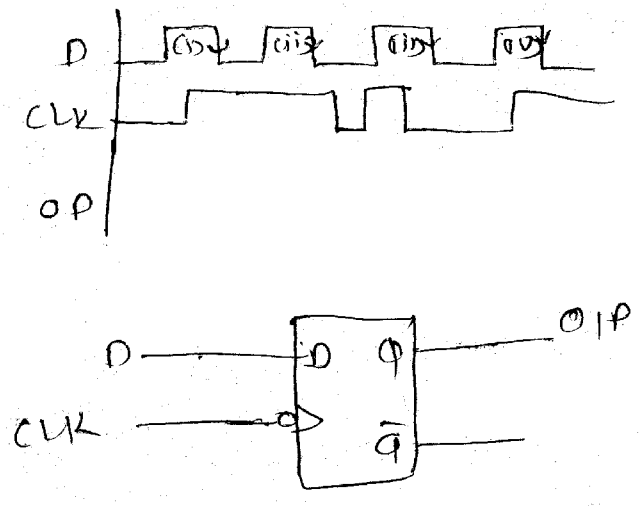

Fig. 2

(b) Convert JK to D flip flop and JK to T flip flop. **5**

(c) Explain positive edge trigger D flip flop. **5**

5 (a) Using JK flip flop design sequential circuit for following state diagram : **8**

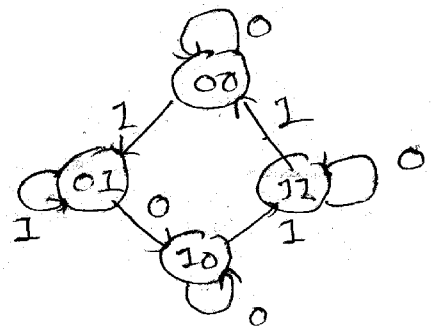

Fig. 4

(b) Explain serial - in serial - out shift register. Draw the diagram for serial - in parallel - out shift register. **7**

OR

5 (a) Reduce the state giagram and give state table for reduced state diagram. **8**

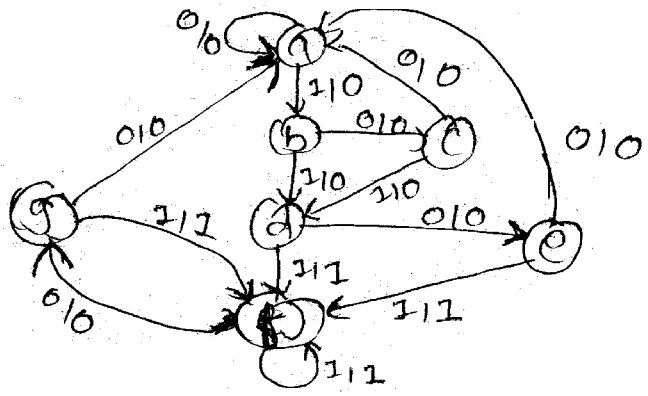

Fig. 5

(b) Design type I synchronous (synchronous counter using T flip flop) that goes through states 0,3,5,6,0.....is the counter self starting. **7**

6 Attempt any **three** : **15**

(a) Explain ring counter and Johnson counter.

(b) Explain in brief ALU with simple example.

(c) Short note on microprogram control for control organization.

(d) Short note on Magnetic core memory.

(e) BCD synchronous counter.